

**WHAT IS CLAIMED IS:**

1. A network switching device for transferring data among  $n$  channels, the network switching device comprising:

$n$  receive circuits each adapted to receive frames of the data from a respective one of the  $n$  channels,

$n$  ingress modules each comprising

a frame data memory controller circuit adapted to store the data of each frame in one or more buffers, wherein each of the buffers is adapted to store a plurality of bytes of the data, and

a destination resolution circuit adapted to select one or more of the  $n$  channels as destination channels for each of the frames;

a forwarding module adapted to enqueue each buffer storing the data of the frames to the respective one or more destination channels;

$n$  egress modules each adapted to transmit, to a respective one of the  $n$  channels, the data in the buffers enqueued to the respective one of the  $n$  channels; and

$n$  counters each adapted to store a count for a respective one of the  $n$  channels, to increment the count when a respective one of the  $n$  ingress modules enqueues a buffer to one or more destination channels, and to decrement the count after the data stored in a buffer enqueued from the respective one of the  $n$  ingress modules is transmitted to one or more of the  $n$  channels to which the buffer was enqueued;

wherein each of the  $n$  egress modules is further adapted to exercise flow control on a respective one of the  $n$  channels when a respective count is greater than a pause threshold.

2. The network switching device of claim 1:

wherein, to exercise flow control, each of the  $n$  egress modules is further adapted to transmit a pause frame to a respective one of the  $n$  channels.

3. The network switching device of claim 2:

wherein each of the  $n$  egress modules is further adapted to terminate flow control on a respective one of the  $n$  channels when the respective count is less than a pause release threshold.

5           4.       The network switching device of claim 3:

wherein, to terminate flow control, each of the  $n$  egress modules is further adapted to transmit a pause release frame to a respective one of the  $n$  channels.

10           5.       The network switching device of claim 2:

wherein, to decrement the count, each of the  $n$  counters is further adapted to decrement the count after the data stored in a buffer enqueued from the respective one of the  $n$  ingress modules is transmitted to all of the  $n$  channels to which the buffer was enqueued.

15           6.       The network switching device of claim 1, further comprising:

$n$  output queues each associated with one of the  $n$  channels and adapted to store pointers for one or more of the buffers; and

wherein, to enqueue one of the buffers to one of the destination channels, the forwarding module is further adapted to send, to the one of the  $n$  output queues associated with the one of the destination channels, a pointer for the one of the buffers.

20           7.       The network switching device of claim 1, further comprising:

$n$  reserve modules each adapted to reserve one or more of the buffers to each of the  $n$  channels;

25           wherein the pause threshold for each of the  $n$  channels is a function of at least one of the group consisting of

the number of the buffers reserved to the channel; and

the number of the buffers neither reserved nor enqueued to any of the  $n$  channels.

30           8.       The network switching device of claim 3, further comprising:

n reserve modules each adapted to reserve one or more of the buffers to each of the n channels;

wherein the pause release threshold for each of the n channels is a function of at least one of the group consisting of

- 5                   the number of the buffers reserved to the channel; and  
                  the number of the buffers neither reserved nor enqueued to any of the n channels.

10           9.     An integrated circuit comprising the network switching device of claim 1.

10.    A network switch comprising the network switching device of claim 1.

11.    The network switching device of claim 1, further comprising:  
15   a memory comprising the buffers.

12.    An integrated circuit comprising the network switching device of claim 11.

13.    A network switching device for transferring data among n channels, the  
20   network switching device comprising:

n receive circuit means for receiving frames of the data from a respective one of the n channels,

n ingress module means for handling the frames of the data, wherein each of the n ingress module means comprises

25           frame data memory controller circuit means for storing the data of each frame in one or more buffers, wherein each of the buffers is adapted to store a plurality of bytes of the data, and

destination resolution circuit means for selecting one or more of the n channels as destination channels for each of the frames;

30           forwarding module means for enqueueing each buffer storing the data of the frames to the respective one or more destination channels;

n egress module means each for transmitting, to a respective one of the n channels, the data in the buffers enqueued to the respective one of the n channels; and

n counter means each for storing a count for a respective one of the n channels, incrementing the count when a respective one of the n ingress module means enqueues a buffer to one or more destination channels, and decrementing the count after the data stored in a buffer enqueued from the respective one of the n ingress module means is transmitted to one or more of the n channels to which the buffer was enqueued;

wherein each of the n egress module means exercises flow control on a respective one of the n channels when a respective count is greater than a pause threshold.

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14. The network switching device of claim 13:

wherein, to exercise flow control, each of the n egress module means transmits a pause frame to a respective one of the n channels.

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15. The network switching device of claim 14:

wherein each of the n egress module means terminates flow control on a respective one of the n channels when the respective count is less than a pause release threshold.

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16. The network switching device of claim 15:

wherein, to terminate flow control, each of the n egress module means transmits a pause release frame to a respective one of the n channels.

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17. The network switching device of claim 14:

wherein, to decrement the count, each of the n counter means decrements the count after the data stored in a buffer enqueued from the respective one of the n ingress module means is transmitted to all of the n channels to which the buffer was enqueued.

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18. The network switching device of claim 13, further comprising:

n output queue means each associated with one of the n channels and for storing pointers for one or more of the buffers; and

wherein, to enqueue one of the buffers to one of the destination channels, the forwarding module means sends, to the one of the  $n$  output queue means associated with the one of the destination channels, a pointer for the one of the buffers.

- 5           19.     The network switching device of claim 13, further comprising:  
               $n$  reserve module means for reserving one or more of the buffers to each of the  $n$   
channels;  
              wherein the pause threshold for each of the  $n$  channels is a function of at least one of  
the group consisting of  
10           the number of the buffers reserved to the channel; and  
              the number of the buffers neither reserved nor enqueued to any of the  $n$   
channels.

20.     The network switching device of claim 15, further comprising:  
15            $n$  reserve module means for reserving one or more of the buffers to each of the  $n$   
channels;  
              wherein the pause release threshold for each of the  $n$  channels is a function of at least  
one of the group consisting of  
              the number of the buffers reserved to the channel; and  
20           the number of the buffers neither reserved nor enqueued to any of the  $n$   
channels.

21.     An integrated circuit comprising the network switching device of claim 13.

- 25           22.     A network switch comprising the network switching device of claim 13.

23.     A method for transferring data among  $n$  channels, the method comprising:  
receiving frames of the data from the  $n$  channels,  
storing the data of each frame in one or more buffers,  
30           selecting one or more of the  $n$  channels as destination channels for each of the frames,  
and

enqueueing each buffer storing the data of the frames to the respective one or more destination channels;

transmitting, to each of the  $n$  channels, the data stored in the buffers enqueueued to the respective one of the  $n$  channels;

5 storing a count for each of the  $n$  channels;

incrementing the count for one of the  $n$  channels when enqueueing a buffer storing data for a frame received by the one of the  $n$  channels;

decrementing the count for one of the  $n$  channels after the data stored in one of the buffers for one of the frames received from the one of the  $n$  channels is transmitted to one or  
10 more of the  $n$  channels to which the one of the buffers was enqueueued;

exercising flow control on one of the  $n$  channels when a respective count is greater than a pause threshold.

24. The method of claim 23, wherein exercising flow control on a respective one  
15 of the  $n$  channels comprises:

transmitting a pause frame to the respective one of the  $n$  channels.

25. The method of claim 24, further comprising:

terminating flow control on one of the  $n$  channels when a respective count is less than  
20 a pause release threshold.

26. The method of claim 25, wherein terminating flow control on a respective one of the  $n$  channels comprises:

transmitting a pause release frame to the respective one of the  $n$  channels.  
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27. The method of claim 24, wherein decrementing the count for one of the  $n$  channels comprises:

decrementing the count after the data stored in the one of the buffers for the one of the frames is transmitted to all of the  $n$  channels to which the one of the buffers was  
30 enqueueued.

28. The method of claim 23, wherein enqueueing one of the buffers to one of the destination channels comprises sending a pointer for the one of the buffers to an output queue associated with the one of the destination channels.

5 29. The method of claim 23, further comprising:  
reserving one or more of the buffers to each of the  $n$  channels;  
wherein the pause threshold for each of the  $n$  channels is a function of at least one of  
the group consisting of  
the number of the buffers reserved to the channel; and  
10 the number of the buffers neither reserved nor enqueued to any of the  $n$   
channels.

30. The method of claim 25, further comprising:  
reserving one or more of the buffers to each of the  $n$  channels;  
15 wherein the pause release threshold for each of the  $n$  channels is a function of at least  
one of the group consisting of  
the number of the buffers reserved to the channel; and  
the number of the buffers neither reserved nor enqueued to any of the  $n$  channels.

20 31. A computer program embodying instructions executable by a processor to  
control an apparatus for transferring data among  $n$  channels, the computer program  
comprising:  
storing the data of each frame received from the  $n$  channels in one or more buffers;  
25 selecting one or more of the  $n$  channels as destination channels for each of the frames;  
enqueueing each buffer storing the data of the frames to the respective one or more  
destination channels;  
causing the apparatus to transmit, to each of the  $n$  channels, the data stored in the  
buffers enqueued to the respective one of the  $n$  channels;  
30 storing a count for each of the  $n$  channels;

incrementing the count for one of the  $n$  channels when enqueueing a buffer storing data for a frame received by the one of the  $n$  channels;

decrementing the count for one of the  $n$  channels after the data stored in one of the buffers for one of the frames received from the one of the  $n$  channels is transmitted to one or  
5 more of the  $n$  channels to which the one of the buffers was enqueued;

causing the apparatus to exercise flow control on one of the  $n$  channels when a respective count is greater than a pause threshold.

32. The computer program of claim 31, wherein causing the apparatus to exercise  
10 flow control on a respective one of the  $n$  channels comprises:

causing the apparatus to transmit a pause frame to the respective one of the  $n$  channels.

33. The computer program of claim 32, further comprising:  
15 causing the apparatus to terminate flow control on one of the  $n$  channels when a respective count is less than a pause release threshold.

34. The computer program of claim 33, wherein causing the apparatus to  
terminate flow control on a respective one of the  $n$  channels comprises:  
20 causing the apparatus to transmit a pause release frame to the respective one of the  $n$  channels.

35. The computer program of claim 32, wherein decrementing the count for one  
of the  $n$  channels comprises:  
25 decrementing the count by after the data stored in the one of the buffers for the one of the frames is transmitted to all of the  $n$  channels to which the one of the buffers was enqueued.

36. The computer program of claim 31, wherein enqueueing one of the buffers to  
30 one of the destination channels comprises sending a pointer for the one of the buffers to an output queue associated with the one of the destination channels.



37. The computer program of claim 31, further comprising:  
reserving one or more of the buffers to each of the  $n$  channels;  
wherein the pause threshold for each of the  $n$  channels is a function of at least one of  
5 the group consisting of  
the number of the buffers reserved to the channel; and  
the number of the buffers neither reserved nor enqueued to any of the  $n$   
channels.

10 38. The computer program of claim 33, further comprising:  
reserving one or more of the buffers to each of the  $n$  channels;  
wherein the pause release threshold for each of the  $n$  channels is a function of at least  
one of the group consisting of  
the number of the buffers reserved to the channel; and  
15 the number of the buffers neither reserved nor enqueued to any of the  $n$  channels.